What is claimed is:

1. A cache formed on an integrated circuit and having a configurable bit that is configurable to identify one of a set having at least one line of information storage and a tag to identify a line of information storage.

2. The cache of claim 1, wherein the cache includes a piece of information, the set includes a plurality of lines in which the piece of information is stored and the tag identifies one of the plurality of lines within the set in which the piece of information is stored.

3. The cache of claim 1, further comprising a second configurable bit, wherein one of the configurable bit and the second configurable bit is configured to identify the set and the other of the configurable bit and the second configurable bit is configured to identify the tag.

4. The cache of claim 1, wherein the cache includes a plurality of lines of information storage and a configurable bit that is configurable to identify one of a set having at least one line of information storage and a tag to identify a line of information storage is associated with each line.

5. The cache of claim 1, wherein the configurable bit is a set index bit when configured to identify the set having at least one line of information storage and the configurable bit is a tag bit when configured to identify the line of information storage.

6. The cache of claim 5, wherein the cache includes a plurality of lines of information storage and each line of information storage includes at least one set index bit.

7. The cache of claim 6 wherein the lines of data storage include no tag bits.

8. The cache of claim 5, wherein the cache includes a plurality of lines of information storage and each line of information storage includes at least one tag bit.

9. The cache of claim 8, wherein the lines of data storage include no set index bits.

10. The cache of claim 5, wherein the configurable bit is configured as a tag bit and reconfigured as a set index bit.

11. The cache of claim 10, wherein all entries in the cache are invalidated prior to reconfiguring the configurable bit so that no address holds valid data prior to the configurable bit being reconfigured as a set index bit.

12. The cache of claim 5, wherein the configurable bit is configured as a set index bit and reconfigured as a tag bit.

13. The cache of claim 12, wherein all entries in the cache are invalidated prior to reconfiguring the configurable bit so that no address holds valid data prior to the configurable bit being reconfigured as a tag bit.

14. The cache of claim 1, further comprising at least a second bit that is configurable to identify one of a set having at least one line of information storage and a tag to identify a line of information storage.

15. A cache formed on an integrated circuit, comprising a bit that is configurable as one of a tag bit and a set index bit.

16. The cache of claim 15, wherein the bit is configurable by movement of a jumper.

17. The cache of claim 15, wherein the bit is configurable through software.

18. The cache of claim 15, wherein the cache includes a plurality of cache lines and further comprising a bit that is configurable as one of a tag bit and a set index bit in each cache line.

19. The cache of claim 15, wherein the bit is reconfigurable from a tag bit to a set index bit.

20. The cache of claim 15, wherein the bit is reconfigurable from a set index bit to a tag bit.

21. A node, comprising:

a processor; and

cache formed on an integrated circuit coupled to the processor to store information for retrieval by the processor, the cache having a configurable bit that is configurable as one of a set index bit and a tag bit.

22. The node of claim 21, wherein the cache includes a plurality of lines of information storage, further comprising a configurable bit that is configurable as one of a tag bit and a set index bit in each line of the cache.

23. The node of claim 21, wherein the configurable bit is reconfigurable from a tag bit to a set index bit.

24. The node of claim 21, wherein the configurable bit is reconfigurable from a set index bit to a tag bit.

25. A method of configuring cache formed on a integrated circuit and having a plurality of address bits, comprising setting at least one of the cache address bits as one of a tag bit and a set index bit.

26. The method of claim 25, wherein the cache includes a plurality of lines and each line includes a plurality of address bits, further comprising setting at least one of the cache address bits in each line of cache as one of a tag bit or a set index bit.

27. The method of claim 25, wherein the cache includes a plurality of information storage locations identified by the address bits, further comprising:

setting at least one of the cache address bits as a tag bit;

placing information in at least one of the information storage locations;

invalidating information in all information storage locations in the cache; and

reconfiguring the bit from a tag bit to a set index bit.

28. The method of claim 25, wherein the cache includes a plurality of information storage locations identified by the address bits, further comprising:

setting at least one of the cache address bits as a set index bit;

placing information in at least one of the information storage locations;

invalidating information in all information storage locations in the cache; and

reconfiguring the bit from a set index bit to a tag bit.

29. An article of manufacture comprising:

a computer readable medium having stored thereon instructions which, when executed by a processor, cause the processor to configure a cache address bit as one of a tag bit and a set index bit.

30. The article of manufacture of claim 29, wherein the cache includes a plurality of lines and each line includes a plurality of address bits, further comprising setting at least one of the cache address bits in each line of cache as one of a tag bit and a set index bit.